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Micro thermoelectric cooler: Planar multistage

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ABSTRACT

A suspended, planar multistage micro thermoelectric (TE) cooler is designed using thermal network model to cool MEMS devices. Though the planar (two-dimensional) design is compatible with MEMS fabrication, its cooling performance is reduced compared to that of a pyramid (three-dimensional) design, due to a mechanically indispensable thin dielectric substrate (SiO_2) and technical limit on TE film thickness. We optimize the planar, six-stage TE cooler for maximum cooling, and predict $\Delta T_{max} = 51$ K with power consumption of 68 mW using undoped, patterned 4–10 μm thick co-evaporated Bi_2Te_3 and Sb_2Te_3 films. Improvement steps of the planar design for achieving cooling performance of the ideal pyramid design are discussed. The predicted performance of a fabricated prototype is compared with experimental results with good agreements.

1. Introduction

A pyramid (three-dimensional), multistage thermoelectric (TE) cooler, as shown in Fig. 1(a), has been studied as a vertically cascaded design for cooling to low temperatures from an ambient, achieving $\Delta T = 50$–100 K [1–3]. Using bulk *n*-type Bi_2Te_3 and *p*-type Sb_2Te_3 TE materials [3], commercialized, six-stage pyramid designs produce $\Delta T = 130$–140 K in a vacuum without an active cooling rate. Previous studies have also proposed planar (two-dimensional) designs to overcome technical challenges of the pyramid (three-dimensional) design for MEMS fabrication processes [2,4–9]. For the planar design, columnar TE couples in the pyramid structure are concentrated at the edges of the dielectric plates of each stage as shown in Fig. 1(b), and collapsed down to build the suspended, planar, concentric thermally isolated structure as shown in Fig. 1(c).

Amongst the past micro TE coolers, a single-stage, pyramid design produced $\Delta T_{max} = 1.3$ K using *n*-type Bi_2Te_3 and *p*-type Sb_2Te_3 films [4], and $\Delta T_{max} = 10.9$ K using *n*-type Bi_2Te_3 and *p*-type $(Bi,Sb)_2Te_3$ films [10], while in [11,12], $\Delta T_{max} = 4.5$ K was achieved using variations of Si and Ge superlattices. For a single-stage, planar design [8], $\Delta T_{max} = 0.76$ K was achieved using InGaAs/InGaAsP superlattices integrated single-stage planar micro cooler, while $\Delta T_{max} = 15.5$ K was measured using a single-stage planar design with *n*-type Bi_2Te_3 and *p*-type Sb_2Te_3 films [13].

However, micro, planar designs carry inherent disadvantages in achieving low temperatures, such as lower thermal isolation caused by additional conduction through dielectric substrate and poor film quality, while pyramid design presents technical challenges for MEMS fabrication processes. Here we design a planar, rectangular, six-stage micro TE cooler using *n*-type Bi_2Te_3 and *p*-type Sb_2Te_3 co-evaporated TE films. A thin, dielectric substrate (SiO_2 film) bridging between thermally isolated islands (Si wafer) is unavoidably included to support TE film couples. Due to their small size (in the order of a few hundred microns) and high thermal conductivity (Si, 150 W/m K), these islands are assumed to be isothermal (i.e., isothermal island). A serpentine tether (glass) is also added to hold the thermal isolation structure. The number of TE couples is the smallest in the last stage (innermost stage), and largest in the first stage (outermost stage) to transport the accumulated heat from the center outward.

In comparison with the pyramid design, there are four significant considerations, namely, thermal isolation, thermal isolation/electrical resistance of the TE film (i.e., optimal TE film dimension aspect ratio including conduction through the substrate and tether), TE film quality, and electrical resistance of inter-connecting electrical wires.

The planar design inherently results in extra thermal conduction paths through the substrate and tether, which in turn decrease

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Nomenclature

ll A_k	cross-sectional area of the thermoelectric element (m^2)
J_e	electrical current (A)
k	thermal conductivity (W/m K)
L	length (m)
N	number of thermoelectric couples
P_e	electrical power (W)
Q	heat flow rate (W)
R_e	electrical resistance (Ω)
R_k	conduction resistance (K/W)
$\dot{S}$	energy conversion rate (W)
T	temperature (K)
w_{te}	width of thermoelectric element (m)
Z_e	figure of merit (1/K)

Greek symbols

α_S	Seebeck coefficient (V/K)
δ	thickness (m)
σ_{SB}	Stefan–Boltzmann constant
ρ_e	electrical resistivity (Ω-m)

Superscripts

amb	ambient
b	boundary
c	cold, contact
e	electrical, electron
ext	extrinsic
h	hot
i	stage, node
int	intrinsic
J	Joule
k	conduction
MEMS	MEMS device
n	*n*-type thermoelectric element, number of stage
opt	optimum
p	*p*-type thermoelectric element or phonon
P	Peltier
r	radiation
s	stage
sub	substrate
te	thermoelectric element
tether	glass serpentine tether
wire	inter-connecting electrical wire

the thermal isolation from the surroundings. Thus, for the optimal design, thermal isolation through those structures should be maximized. In addition, direct exposure of the cooler structure to surroundings allows for an increase in radiation, especially for large temperature difference between the cold stage and the surroundings. Also, the substrate thickness controls the optimal ratio of thermal conduction resistance to electrical resistance. While the optimal dimension aspect ratio of TE couples changes with the substrate thickness, it remains constant without the substrate because it is determined only by TE film material properties [2]. For co-evaporated *n*-type Bi_2Te_3 and *p*-type Sb_2Te_3 TE films, lower Seebeck coefficient and higher electrical resistivity are measured than those of bulk TE materials [6,14,15]. The thermal conductivity of thin-film, in general, is lower than the bulk value, since large grain boundary scattering of thin-film hinders phonon transport [16]. For a conservative estimate, we use the same thermal conductivity for TE films as that of bulk TE materials [6,13]. Thus, the TE figure of merit of TE films is expected to be lower than that of bulk TE elements, which in turn decreases cooling performances. Micro sized inter-connecting electrical wires also lower cooling capability by increasing Joule heating and by providing additional thermal paths. A comparison between the planar and pyramid designs is given in Table 1.

In Section 2, we discuss intrinsic (only material) and extrinsic (material and geometry) TE figures of merit for a multistage cooler, and in Section 3, we develop a thermal network model that includes interfacial phenomena. In Section 4, we compare predictions with on-going experimental results, and discusses the optimal planar six-stage design and improvements to reach cooling performances of an ideal pyramid design.

Details of MEMS fabrication processes for the planar, multistage micro cooler are found in [17], and discussions of TE film deposition are also given in [14,15].

2. Thermoelectric figure of merit

The intrinsic (material only) thermoelectric figure of merit including both *n*- and *p*-type TE materials is defined as [18]

$$Z_{e,int} \equiv \frac{\alpha_S^2}{\left[(k\rho_e)_p^{1/2} + (k\rho_e)_n^{1/2}\right]^2}, \tag{1}$$

where α_S is the junction Seebeck coefficient (i.e., $\alpha_S = \alpha_{S,p} - \alpha_{S,n}$), k is the total thermal conductivity which is a sum of phonon k_p and electronic k_e thermal conductivity (i.e., $k = k_p + k_e$), and ρ_e is the electrical resistivity.

Including the geometries of the TE couples, dielectric substrate, glass tether, and inter-connecting electrical wires, we define the extrinsic (material and geometry) thermoelectric figure of merit as

$$Z_{e,ext} = \frac{\alpha_S^2}{R_e/R_k}, \tag{2}$$

where the thermal resistance R_k, and the electrical resistance R_e. These are

$$\begin{aligned}
R_k &= \sum_{i=1}^{N_s} R_{k,i} \\
R_e &= \sum_{i=1}^{N_s} (R_{e,te,i} + R_{e,wire,i}) \\
\frac{1}{R_{k,i}} &= \frac{1}{R_{k,te,i}} + \frac{1}{R_{k,sub,i}} + \frac{1}{R_{k,tether,i}} \\
\frac{1}{R_{k,te,i}} &= N_i\left[\frac{1}{(R_{k,te})_p} + \frac{1}{(R_{k,te})_n}\right] = N_i\left[\left(\frac{A_{k,te}k}{L_{te}}\right)_p + \left(\frac{A_{k,te}k}{L_{te}}\right)_n\right] \\
R_{e,te,i} &= N_i\left[\left(\frac{\rho_e L_{te}}{A_{k,te}}\right)_p + \left(\frac{\rho_e L_{te}}{A_{k,te}}\right)_n\right].
\end{aligned} \tag{3}$$

In Eq. (3), N_s is the number of the stage, N_i is the number of TE couples in the ith stage, $R_{k,te,i}$ is the thermal resistance of the TE material at the ith stage, $R_{k,sub,i}$ the thermal resistance of substrate at the ith stage, $R_{k,tether,i}$ is the thermal resistance of glass tether at the ith stage, $R_{e,te,i}$ is the electrical resistance of TE material at the ith stage, and $R_{e,wire,i}$ is the electrical resistance of inter-connecting

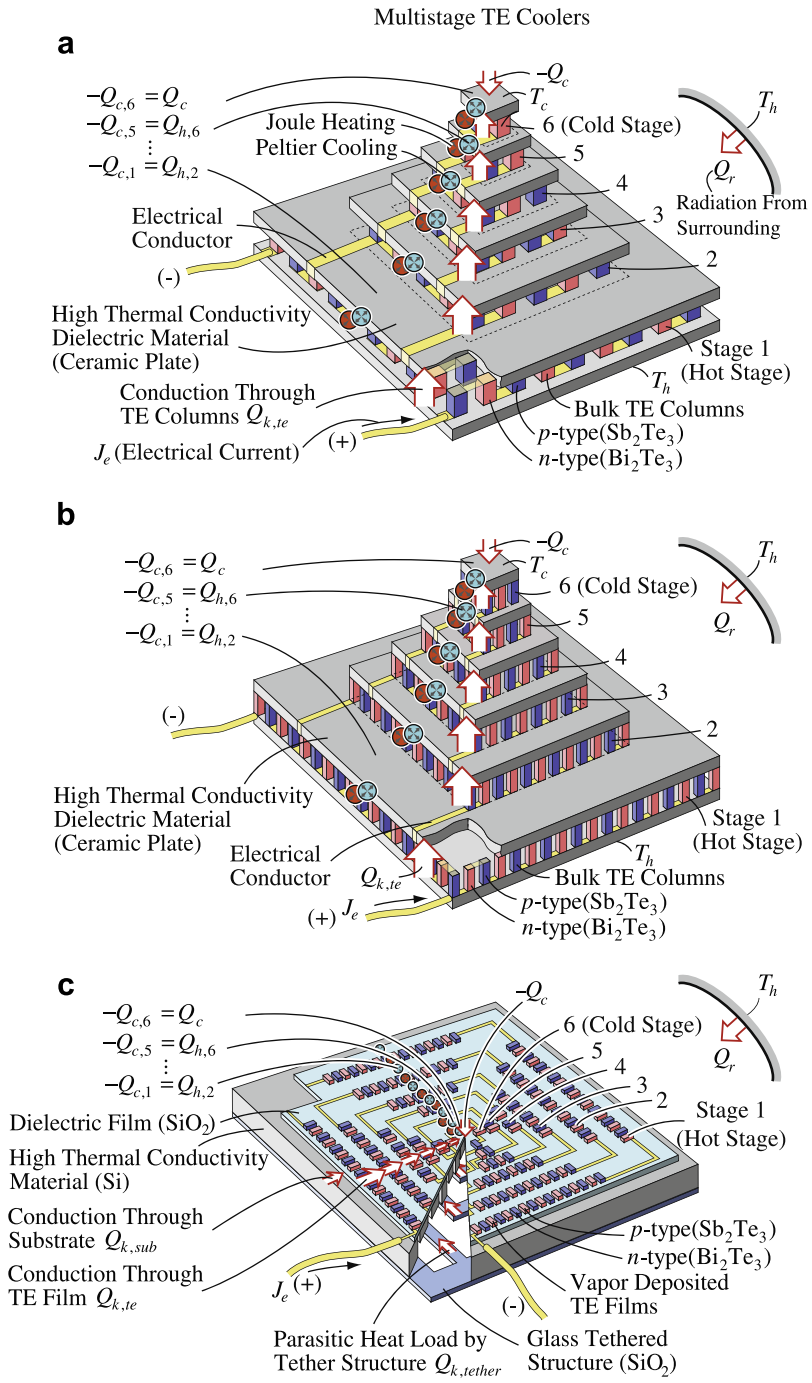

Fig. 1. Schematics of six-stage TE coolers. (a) Pyramid (three-dimensional) design using bulk TE couples spaced the dielectric stages, (b) pyramid (three-dimensional) design using bulk TE couples arranged on the periphery, and (c) planar (two-dimensional) design using TE films including a thin substrate and a serpentine glass tether. Thermal conduction and radiation, heat sources/sinks, *n*- and *p*-type TE elements, inter-connecting electrical wires, hot, and cold stage temperatures are also shown.

Table 1
Comparison between multistage planar and pyramid designs.

	Planar	Pyramid
Thermal isolation	Radiation for the inner stages is not isolated from surroundings	Each stage is fully isolated by thin plates, thus preventing radiation from penetration
	Conduction through TE films and their substrates	Conduction only through TE couples
TE couple structure	Thin TE films supported by dielectric substrate connecting stages	Spaced columnar couples filling the space between stages
	Material properties and substrate thickness dependent optimal TE aspect ratio	Only material properties dependent optimal TE aspect ratio
TE element	Vapor deposited *n*-type Bi_2Te_3, *p*-type Sb_2Te_3 [14,15]	Bulk *n*-type Bi_2Te_3, *p*-type Sb_2 Te_3 [3]
Resistance of inter- connecting electrical wires	Significant	Negligible

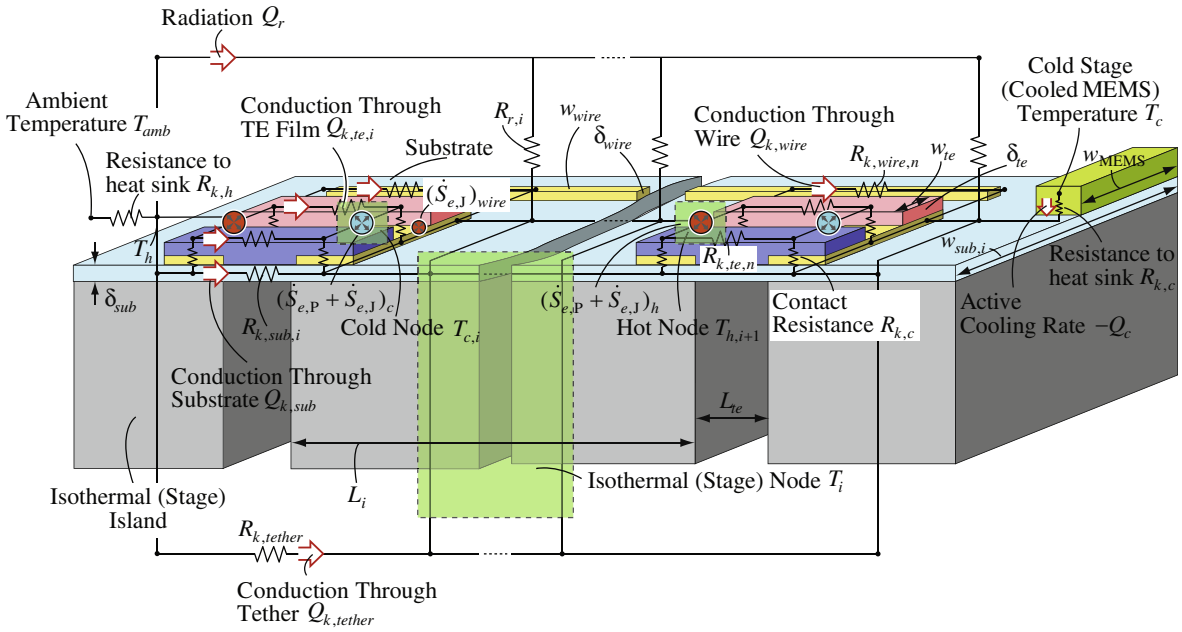

Fig. 2. Thermal circuit diagram for planar multistage micro cooler. It includes Peltier cooling/heaing, Joule heating, thermal conduction, thermal radiation, and interfacial thermal/electrical resistances. Three temperature nodes are marked at the isothermal (stage) node T_i, cold $T_{c,i}$ and hot $T_{h,i+1}$ junctions of TE couples. The cold stage temperature T_c (cooled MEMS) and ambient (surrounding) temperature T_{amb} are also shown.

wires at the ith stage. These resistances are shown in Fig. 2. For an ideal pyramid design, no substrate and no tether are allowed, so $R_{k,sub,i} \to \infty$, and $R_{k,tether,i} \to \infty$. Also, $R_{e,wire,i} \to 0$, because the electrical resistances of inter-connecting wires are negligibly small.

The thermoelectric figure of merit signifies the efficiency of TE devices. The active cooling rate Q_c at the optimal current $J_{e,opt}$ is given as [18]

$$-Q_c = \frac{1}{R_k}\left[\frac{Z_{e,ext}T_c^2}{2} - (T_h - T_c)\right], \quad J_{e,opt} = \frac{\alpha_S T_c}{R_e}. \tag{4}$$

The maximum temperature difference ΔT_{max}, between the hot stage temperature T_h and cold stage temperature T_c, for $Q_c = 0$ is [18]

$$\Delta T_{max} \equiv (T_h - T_c)_{max} = \frac{Z_{e,ext}T_c^2}{2}. \tag{5}$$

To maximize ΔT_{max}, large extrinsic thermoelectric figure of merit $Z_{e,ext}$ is needed, which is achieved by increasing film quality $Z_{e,int}$ and by optimizing the structure. Discussions on improving $Z_{e,int}$ are found in [14,15,19], and we will optimize the design by improving the thermal isolation and reducing the electrical resistance.

3. Thermal network model

To elucidate and analyze the multistage TE micro cooler, a thermal network model is developed considering the Peltier cooling/heating, Joule heating, thermal conduction, thermal radiation, and temperature dependent TE material properties, as shown in Fig. 2. The hot stage temperature T_h, [leftmost temperature junction, or outermost temperature junction in Fig. 1(c)] which is exposed to the ambient temperature T_{amb}, is thermally and electrically connected by TE couples (including the substrate) with the next-stage temperature junction T_i. This continues for the second stage, etc. up to the cold stage temperature T_c [cooled MEMS site (rightmost), or the innermost stage in Fig. 1(c)].

Peltier cooling/heating, $(\dot{S}_{e,P})_c$, $(\dot{S}_{e,P})_h$ are considered at cold/hot junctions of each set of TE couple. Thermal conduction resistance, R_k includes TE couples, thin substrate, tether, inter-connecting electrical wires as well as thermal boundary/contact resistances. Thermal radiation resistance, R_r consists of radiation exchanges between the surroundings and each stage. Joule heating results from TE couples, inter-connecting electrical wires, and electrical contacts. Detailed discussions concerning the thermal/electrical boundary/contact resistances as an interfacial transport are found in [20]. Convection is neglected due to ancipated vacuum packaging [17].

Under steady-state condition, the energy equation for thermal node i, as shown in Fig. 2, is [21]

$$Q|_{A_i} = \sum_j \dot{S}_j, \tag{6}$$

where $Q|_{A_i}$ is the net heat transfer through the surface A_i, and $\dot{S}_j$ is the nodal energy conversion, which comprises Peltier cooling/heating, or Joule heating. For the temperature node T_i, Eq. (6) becomes

$$Q_{c,i} - Q_{h,i+1} + \sum_j Q_{k,sub,j} + \sum_j Q_{k,wire,j} + \sum_j Q_{k,tether,j} + \sum_j Q_{r,j} = (\dot{S}_{e,J})_{wire,i} \quad \text{at temperature node } T_i, \tag{7}$$

where $Q_{c,i}$ is the heat transfer at the cold junction of the TE couples in the ith stage, $Q_{h,i+1}$ is the heat transfer at the hot junction of the TE couples in the $(i+1)$th stage, $Q_{k,sub}$ is the conduction through the substrate, $Q_{k,wire}$ is the conduction through the inter-connecting electrical wires, $Q_{k,tether}$ is the conduction through the tether, Q_r is the radiation exchange with the surroundings, $(\dot{S}_{e,J})_{wire,i}$ is the Joule heating by the inter-connecting electrical wires.

For the hot and cold temperature nodes of TE couples at each stage $T_{c,i}$, $T_{h,i+1}$, respectively, the energy equations are

$$-Q_{c,i} + Q_{k,te,i} = (\dot{S}_{e,P} + \dot{S}_{e,J})_{c,i} \text{ at cold node of TE couples} T_{c,i} \tag{8}$$

$$Q_{h,i+1} + Q_{k,te,i+1} = (\dot{S}_{e,P} + \dot{S}_{e,J})_{h,i+1} \text{ at hot node of TE couples} T_{h,i+1}, \tag{9}$$

where $Q_{k,te,i}$ is conduction through the TE couples, $\dot{S}_{e,P}$ is the Peltier cooling/heating, and $(\dot{S}_{e,J})_{c/h}$ is the Joule heating either at the cold or hot junction of the TE couples. These are

$$Q_{k,te,i} = \frac{(T_{h,i} - T_{c,i})}{R_{k,te,i}}, \quad Q_{k,sub,i} = \frac{(T_i - T_{i-1})}{R_{k,sub,i}},$$

$$Q_{k,wire,i} = \frac{(T_i - T_{i-1})}{R_{k,wire,i}}, \quad Q_{r,i} = \frac{\sigma_{SB}(T_{amb}^4 - T_i^4)}{R_{r,i}},$$

$$\dot{S}_{e,J} = \frac{1}{2}R_{e,te,i}J_{e,i}^2, \quad (\dot{S}_{e,P})_c = -\alpha_S J_{e,i}, (\dot{S}_{e,P})_h = \alpha_S J_{e,i+1},$$

where $T_{h,i}$ and $T_{c,i}$ are the temperatures at the hot/cold junctions at the ith stage, $R_{k,te,i}$ is the thermal resistance of the TE couples, $R_{k,sub,i}$ is the thermal resistance of the substrate, $R_{k,wire,i}$ is the thermal resistance of the inter-connecting electrical wires, σ_{SB} is the Stefan–Boltzmann constant, $R_{e,i}$ is the electrical resistance, and $J_{e,i}$ is the electrical input current in the ith stage.

For the outermost and innermost temperature nodes, the energy equations become

$$Q_{h,1} = \frac{T_h - T_{amb}}{R_{k,h}} \tag{10}$$

$$-Q_{c,n} = \frac{T_c - T_n}{R_{k,c}} = -Q_c + \sum_j Q_{r,n,j} - Q_{k,tether,n}, \tag{11}$$

where $R_{k,h}$ and $R_{k,c}$ are the thermal resistances at the hot-end and cold-end heat sinks respectively, and $-Q_c$ is the active cooling rate for MEMS device. The ambient temperature T_{amb} is set to 300 K, and T_h is predicted nearly the same as T_{amb}.

4. Results and discussions

4.1. Predictions and experimental data

The predictions using the thermal network model are compared with the on-going experimental results of a planar, five-stage prototype [17] as shown in Fig. 3. The cold stage temperatures and power consumptions are measured, while varying the electrical current. With a temperature measurement uncertainty of ±5% [17], this cooler produces maximum cooling of $\Delta T_{max} = 9$ K, with the electrical power consumption of $P_e = 12$ mW. The predicted electrical power consumptions and optimal electrical current where the minimum cooling temperature occurs, agree with the experimental data within the range of uncertainty. Considering a measurement uncertainty of the substrate thickness and a lack of measurements of k, two estimated values for a substrate thickness and a cross-plane thermal conductivity k of TE film are used. Within a substrate thickness measurement uncertainty, the value of k fitted to $Z_{e,int}T$ ($T = 300$ K) = 0.62, is $k = 1.0$ W/m K. The predicted cold stage temperatures T_c show good agreement with the measurements. Based on this, in the following analysis, we use the measured TE film values for α_S and ρ_e, along with k fitted to $Z_{e,int}T$ ($T = 300$ K) = 0.62.

4.2. Optimal design

To achieve the maximum cooling, the extrinsic TE figure of merit in Eq. (2) should be maximized. The optimization parameters are:

(a) TE couple dimension aspect ratio (i.e., width of TE element w_{te} for given length L_{te} and thickness δ_{te}),
(b) electrical current $J_{e,i}$, and its stage ratio $J_{e,i}/J_{e,i+1}$, and
(c) number of TE couples in the last stage, N_6, and ratio of number of TE couples in adjacent stages, N_i/N_{i+1}.

For TE couples, the ratio of the cross-section area $A_{k,te}$ to the length L_{te} [Eq. (3)] determines the thermal and electrical resistance of TE elements. A long element with a small cross-section area allows for high thermal isolation, while a short element with a large cross-section area provides a low electrical resistance. Since the TE film thickness is limited by co-evaporated deposition technique, $\delta_{te,max} \leqslant 10$ μm, only its length and width are optimized. A similar approach was used in [20]. Here, we use $\delta_{te} = 4$ μm with MEMS cooler device size of $w_{sub} = 5500$ μm, and optimize TE film width w_{te} (given $J_{e,6}$, $J_{e,i}/J_{e,i+1}$, N_6, and N_i/N_{i+1}). Fig. 4 shows variation of T_c with respect to w_{te} for subject to geometric constraint dimension (packing limit at first stage, N_1) for given device size ($w_{te,max} = 120$ μm for $w_{sub} = 5500$ μm). T_c decreases as w_{te} increases, since the larger cross-section area A_{te} reduces the Joule heating. The minimum T_c is predicted at $w_{te} = 120$ μm. Here, we set $w_{te} = 120$ μm as geometric constraint.

A moderate electrical current favors the Peltier cooling, while excessive current results in Joule heating. Note that the optimal electrical current $J_{e,opt}$ is given in Eq. (4). The electrical current supply can be in series or in parallel for each stage. Even though the parallel arrangement has an advantage in supplying optimal electrical currents for each stage, it adds multiple (parallel) thermal

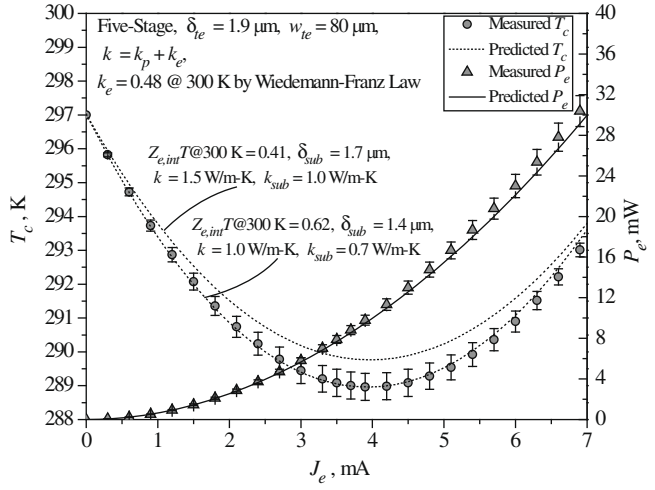

Fig. 3. Comparison between the predicted and the measured cold stage temperatures, and power consumptions of a planar five-stage prototype [17]. The predictions are for two values of TE film thermal conductivity. The prototype specifications are also shown.

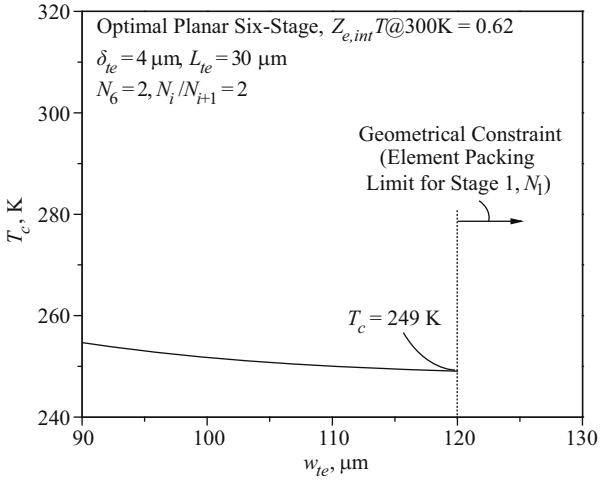

Fig. 4. Variation of the predicted cold stage temperature of the optimal planar six-stage micro TE cooler, as a function of TE element width w_{te}, using TE film with $Z_{e,int}T = 0.62$. The detailed specifications are found in Tables 2 and 3. The geometrical constraint is also marked.

paths which in turn compromise the thermal isolation. Based on the thermal network model predictions using such complex electrical current supply, the parallel arrangement produces only small enhancement in the cold stage temperature. A similar prediction is also found in [1]. Thus, only the serial arrangement is considered here ($J_i/J_{i+1} = 1$). Table 2 lists the range of geometric parameters used in the optimization, and Table 3 lists the thermal conductivities, electrical resistances, and surface emissivities used. The temperature-dependent TE film properties (fitted) are also given (measured values are reported in [15]).

The number of TE couples of the innermost stage N_6, is important, since it contributes the most to the thermal isolation between the cold stage and surroundings, and Joule heating by the innermost stage results in heat loads for the lower stages. While using a large number of TE couples improves Peltier cooling in the innermost stage, the overall cooling performance diminishes. This is due to the reduced thermal isolation and increased Joule heating for the lower stages. Thus, the smallest number of TE couples is desirable in the innermost stage, and it is predicted that only one TE couple produces the best performance. However, an even number should be used to minimize mechanical (structural) damage from asymmetric thermal stress [17]. Here, two TE couples are used in the innermost stage, i.e., $N_6 = 2$. The ratio of TE couples over the stages is also critical to the cooling power because it controls the thermal isolation and total electrical resistance. While a large number ratio yields increased Peltier cooling, it produces decreased thermal isolation and increased Joule heating. TE couple arrangements at each stage should be symmetric to minimize mechanical damages from an asymmetric thermal stress. With these considerations and the optimization approach mentioned above, the thermal network model using conjugate-gradient minimization predicts the optimal ratio of the TE couples $N_i/N_{i+1} = 2$, as shown in Fig. 5. It is close to the optimal design structure studied in an ideal four-stage cooler [1].

Table 2
Geometrical parameters for the optimal planar six-stage design.

Parameter		Description	Magnitude
Isothermal islands (Bulk Si)	w_{MEMS}	One edge length of MEMS die	1500 μm
	L_i	Width of isothermal island ($j = 1,\ldots,6$)	250–750 μm
	δ_i	Thickness of isothermal island ($j = 1,\ldots,6$)	300 μm
TE films	L_{te}	Length of TE couples	30 μm
	$w_{te,i}$	Width of TE couples in ith	120 μm
	δ_{te}	Film thickness of TE couples	4 μm
Number of TE couples	N_6	Number of TE couples in the last (innermost) stage	2
	N_i/N_{i+1}	Number ratio of TE couples between stages ($j = 1,\ldots,5$)	2
	N_1	Number of TE couples in the first (outermost) stage	64
Substrate (SiO_2 film)	L_{sub}	Length of thin substrate over stage	30 μm
	w_{sub}	Width of thin substrate	1,500–5,500 μm
	δ_{sub}	Thickness of thin substrate	1.5 μm
Electrodes	L_{elec}	Length of electrode between TE couples	50 μm
	w_{elec}	Width of electrode	100 μm
	δ_{elec}	Thickness of electrode	0.5 μm
Wire	L_{wire}	Length of electrical wire	1,000–4,000 μm
	w_{wire}	Width of electrical wire	10–100 μm
	δ_{wire}	Thickness of electrical wire	0.5 μm

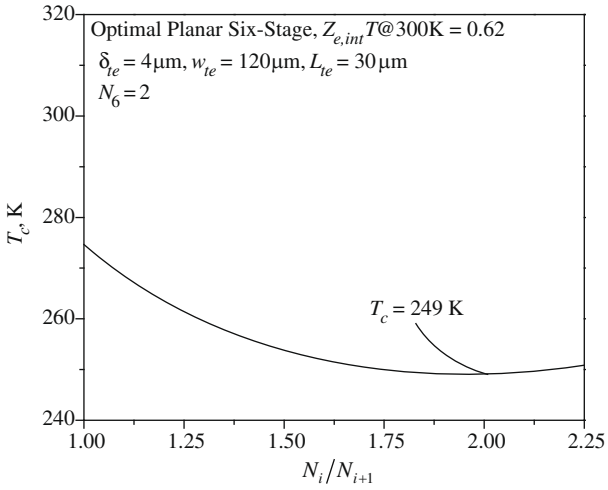

Fig. 5. Variation of the predicted cold stage temperature of the optimal planar six-stage micro TE cooler, as a function of the ratio of number of TE couples N_i/N_{i+1}, using TE film with $Z_{e,int}T = 0.62$. Detailed specifications are found in Tables 2 and 3.

Table 3
Material properties used for the optimal planar six-stage design.

Parameter		Description	Magnitude
Thermal properties	$k_{te,n}$	Thermal conductivity of n-type TE film [20]	1.0 W/m K
	$k_{te,p}$	Thermal conductivity of p-type TE film [20]	1.0 W/m K
	k_{sub}	Thermal conductivity of substrate [24]	0.7 W/m K
	k_{wire}	Thermal conductivity of electrical gold wire [25]	200 W/m K
	ϵ_1	Emissivity of packaging shell [21]	0.1
	ϵ_2	Emissivity of silicon wafer [21]	0.9
Thermal/electrical boundary/contact resistances	$(A_kR_k)_c$	Thermal contact resistance [20]	1×10^{-7} K/(W/m^2)
	$(A_kR_e)_c$	Electrical contact resistance [17]	4.6×10^{-11} Ω m^2
	$(A_kR_k)_{b,n}$	Total boundary resistance at n-type TE [20]	7.2×10^{-8} K/(W/m^2)
	$(A_kR_k)_{b,p}$	Total boundary resistance at p-type TE [20]	7.4×10^{-8} K/(W/m^2)
Resistances to heat sinks	$R_{k,h}$	Thermal resistances to an ambient from hot stage [21]	10 K/W
	$R_{k,c}$	Thermal resistances to the innermost stage from cold stage [21]	10 K/W

For temperature-dependent (fitted) α_S and ρ_e are (measured values are reported in [15]),

$$\alpha_{S,n} = (-7.715 - 0.8607T_{avg} - 7.535 \times 10^{-4}T_{avg}^2 + 4.596 \times 10^{-6}T_{avg}^3) \times 10^{-6},$$

$$\alpha_{S,p} = (94.91 - 0.3018\,T_{avg} + 3.840 \times 10^{-3}T_{avg}^2 - 7.053 \times 10^{-6}T_{avg}^3) \times 10^{-6},$$

$$\rho_{e,n} = (5.740 - 0.04166\,T_{avg} + 4.999 \times 10^{-4}T_{avg}^2 - 6.756 \times 10^{-7}T_{avg}^3) \times 10^{-6},$$

$$\rho_{e,p} = (8.651 - 0.01255\,T_{avg} + 1.505 \times 10^{-4}T_{avg}^2 - 1.813 \times 10^{-7}T_{avg}^3) \times 10^{-6},$$

where $T_{avg} = (T_{c,i} + T_{h,i})/2$.

The predicted cold stage temperatures and power consumptions in the optimal planar six-stage TE cooler with respect to the electrical current are shown in Fig. 6. The optimal design achieves $\Delta T_{max} = 51$ K with power consumption of $P_e = 68$ mW. This prediction is considered as a baseline design for the improvements in Section 4.3.

When the cooling rate $Q_c \neq 0$ [Eq. (4)], the optimal TE cooler design is different from the design for ΔT_{max}. The $Q_c \neq 0$ decreases ΔT because it consumes the Peltier cooling capability, and the reduced ΔT allows for lower thermal isolation from the surroundings. The reduced thermal isolation R_k is beneficial for decreased Joule heating (due to increased cross-section area of TE elements i.e., low R_e). Thus, from Eq. (4), the optimal design for $Q_c \neq 0$ requires reduced thermal resistance R_k, increased $Z_{e,ext}$, and minimum $T_h - T_c$. The reduced R_k in multistage cooler is obtained by an increase in the number of TE elements of each stage and the enlarged width of each element (for given $Z_{e,ext}$, and $T_h - T_c$).

4.3. Improvements

The micro planar TE cooler has several inherent disadvantages due to film deposition constraints and intrinsic structural requirements, which are not present in an ideal pyramid design. These are, (a) poorer film quality $Z_{e,int}$, (b) thinner TE film thickness δ_{te}, (c) greater substrate thickness δ_{sub}, (d) higher electrical wire resistances $R_{e,wire}$, (e) higher interfacial resistances $R_{k,c}$, $R_{e,c}$, and (f) higher radiation Q_r. The benefits from each sequential thermal/electrical improvements for the above factors (a) to (f) are studied in the planar six-stage design, and are described by design designations 1–6 as listed in Table 5. The baseline design is the predicted optimal planar six-stage TE cooler discussed in Section 4.2. Design 1 uses bulk TE properties $Z_{e,int}T$ ($T = 300$ K) = 0.74 [3], and Design 2 uses thicker TE film $\delta_{te} \rightarrow 15\mu$m, Design 3 remove the substrate $\delta_{sub} \rightarrow 0$. Design 4 eliminates the inter-connecting electrical wire resistances $R_{e,wire} \rightarrow 0$, Design 5 removes thermal/electrical contact resistances $R_{k,c} \rightarrow 0$, $R_{e,c} \rightarrow 0$, and Design 6 eliminates radiation heat gain $Q_r \rightarrow 0$. For the ideal design, the design without any disadvantages [above (a) to (f)] of the planar design, whose cold stage temperature is close to that of the commercially available six-stage pyramid macro cooler, is used for comparison and ideally improved design.

Using design specifications given in Table 4, and the bulk TE n-type Bi_2Te_3 and p-type Sb_2Te_3 with $Z_{e,int}T$ ($T = 300$ K) = 0.74 [3], the cold stage temperature T_c is predicted by thermal network model as shown in Fig. 7. A $\Delta T_{max} = 127$ K is predicted at the optimal electrical current $J_{e,opt} = 5$ A. This is in line with the commercially available units. For the six-stage micro pyramid cooler (described in Table 2) gives a $\Delta T_{max} = 130$ K (or $T_c = 170$ K) for $Z_{e,int}T$ ($T = 300$ K) = 0.74, and it is considered as the ideal micro pyramid design, which is an ideally improved reference design. The reason for the better performance of this ideal micro pyramid design by $\Delta T_c = 3$ K is its further optimization of the ratio of number of TE couples in adjacent stages, N_{i+1}/N_i as shown in Tables 2 and 4.

Variations of the predicted cold stage temperature, with respect to electrical current, of all the design variations including the baseline and ideal pyramid design are shown in Fig. 8. Design 1 using

Table 4
Geometrical parameters for the commercially available pyramid six-stage macro design (Fig. 7).

Parameter		Description	Magnitude
TE columns	L_{te}	Length of TE couples	1.8 mm
	w_{te}	Width of TE square section element	2.0 mm
Number of TE couples in each stage	N_6	Number of TE couples in stage 6	1
	N_5	Number of TE couples in stage 5	2
	N_4	Number of TE couples in stage 4	4
	N_3	Number of TE couples in stage 3	9
	N_2	Number of TE couples in stage 2	21
	N_1	Number of TE couples in stage 1	49

Table 5
Summary of specifications for improved planar design towards pyramid (optimal) design. The design numbers are those marked in Fig. 8.

Design	TE Properties	δ_{te}, μm	δ_{sub}, μm	$R_{e,wire}$	$R_{e,c}$,$R_{k,c}$	Q_r
Baseline Planar	Film [15]	4	1.5	○	○	○
Design 1	Bulk [3]	4	1.5	○	○	○
Design 2	Bulk	15	1.5	○	○	○
Design 3	Bulk	15	0	○	○	○
Design 4	Bulk	15	0	×	○	○
Design 5	Bulk	15	0	×	×	○
Design 6	Bulk	15	0	×	×	△
Ideal Pyramid	Bulk	15	0	×	×	△

○ existing, × removed, △ reduced.

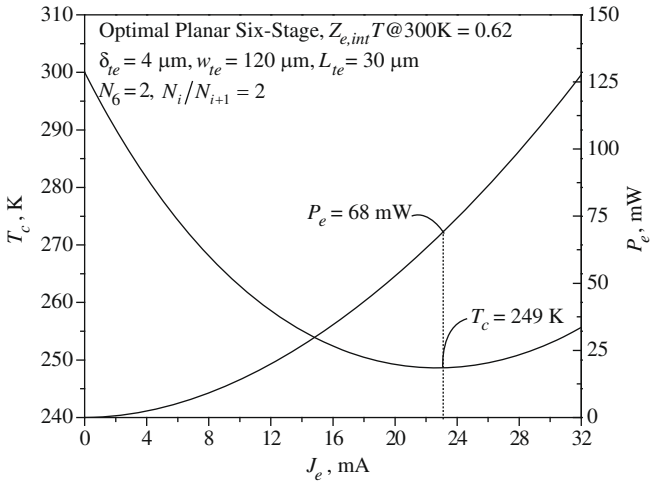

Fig. 6. Variation of the predicted cold stage temperature and power consumption of the optimal planar six-stage micro TE cooler, with respect to electrical current using TE film with $Z_{e,int}T = 0.62$. The detailed specifications are found in Table 2 and 3.

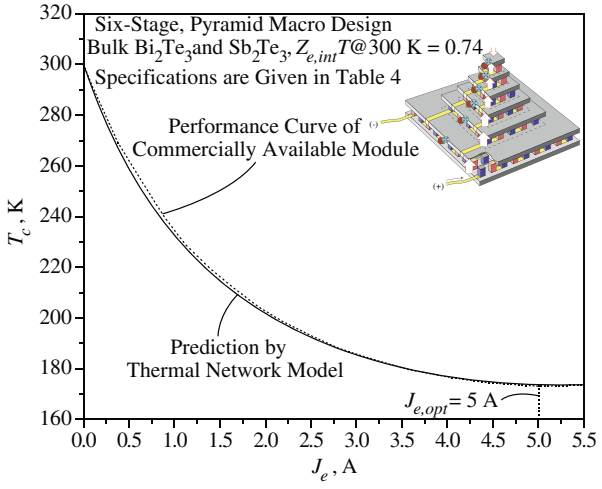

Fig. 7. Predicted cold stage temperature using the thermal network model for $Z_{e,int}T$ ($T = 300$ K) = 0.74 [3] of the macro pyramid design. The optimal electrical current $J_{e,opt} = 5$ A, is also shown. Detailed specifications are given in Table 4.

bulk TE couples, $Z_{e,int}T$ (T = 300 K) = 0.74, shows further cooling of ΔT = 20 K. Design 2 manipulates the denominator in Eq. (2) by increasing TE film thickness, and it is predicted that δ_{te} = 15 μm is the optimal TE thickness which results in further ΔT = 6 K cooling at higher electrical current. The higher optimal input current is caused by reduction in TE film electrical resistance in Eq. (5). In Design 3, it is assumed that the thin SiO_2 substrate and the glass tether are removed, and it produces further ΔT = 14 K. The TE film quality, thickness, and substrate thickness are critical to cooling performances, which we will discuss these in the following subsections (A)–(C). Without Joule heating by the electrical wires in Design 4, an additional ΔT = 32 K can be achieved. In Designs 5 and 6, the interfacial resistances and radiation are reduced, and the results show that these are not critical parameters. For the further improvement, only one TE couple in the innermost stage will result in an additional cold stage temperature ΔT = 4 K. Therefore, if the inherent technical challenges mentioned above are resolved in the planar design, the maximum temperature difference will be increased by nearly 2.6-fold.

(A) Thermoelectric Film Properties $Z_{e,int}T$: Improved TE film quality enhances cooling performance in a micro TE cooler. The film properties are discussed in [13–15]. Fig. 9 shows variation of the predicted cold stage temperature T_c for $Z_{e,int}T$ (T = 300 K) values of 0.41 (film, using bulk k = 1.5 W/m K), 0.62 (film, using fitted film k = 1.0 W/m K), and 0.74 (bulk) [3]. For $Z_{e,int}T$ = 0.41, ΔT_{max} = 39 K is predicted, and with $Z_{e,int}T$ = 0.62 a further ΔT = 12 K is calculated. Using $Z_{e,int}T$ = 0.74, improvement of ΔT = 20 K at an increased optimal input current is achieved by decreasing electrical resistance, improving Seebeck coefficient, or decreasing the thermal conductivity. Note that the cooling performance is not proportional to $Z_{e,int}T$ which does not include geometries. This is caused by different contributions of $Z_{e,int}T$ to the thermal and electrical resistances in Eq. (2) for given geometries. Further improvement in $Z_{e,int}T$ would be desired (i.e., superlattices [22] or alloys [23]).

(B) Substrate Thickness δ_{sub}: Maximizing thermal isolation of the structure by removing the substrate thickness and tether yields improved cooling performance. Fig. 10 shows that cold stage temperatures for substrate thicknesses of 0 and 1.5 μm, and with and without thermal resistance of the glass tether, $R_{k,tether}$ = 15,000 K/W [17] as a function of input current. When the substrate is completely removed $\delta_{sub} \rightarrow 0$, keeping the glass tether, a further ΔT = 11 K is achieved at a similar optimal input current. When, in addition, the glass tether is removed, an extra ΔT = 5 K is gained at a similar optimal input current. This is because the fully suspended TE structure maximizes thermal isolation.

(C) Thermoelectric Film Thickness δ_{te}: Achieving an optimal ratio of R_e to R_k in Eq. (2) by manipulating TE film thickness produces improved cooling performance. Here we limit the TE film thickness to δ_{te} = 4–15 μm, and use δ_{sub} = 1.5 μm for our baseline design. Fig. 11 shows the variations of the cold stage temperature, with respect to input current, for δ_{te} = 4, 10, 15, and with given δ_{sub} = 1.5 μm. Thicker TE films improve cooling performance, and a further ΔT = 7 K is predicted for δ_{te} = 15 μm. Fig. 12 shows the cold stage temperatures as a function of TE film thickness. The cold stage temperatures increase sharply as the TE film thickness is reduced, and then reach the asymptotic cold stage temperature for large δ_{te}, where conduction through the substrate is negligible compared to that through the TE film. As the substrate thickness decreases, the cold stage temperature is also reduced and it results in ΔT = 12 K, when the substrate is completely removed. A decreased substrate thickness results in a thinner asymptotic TE film

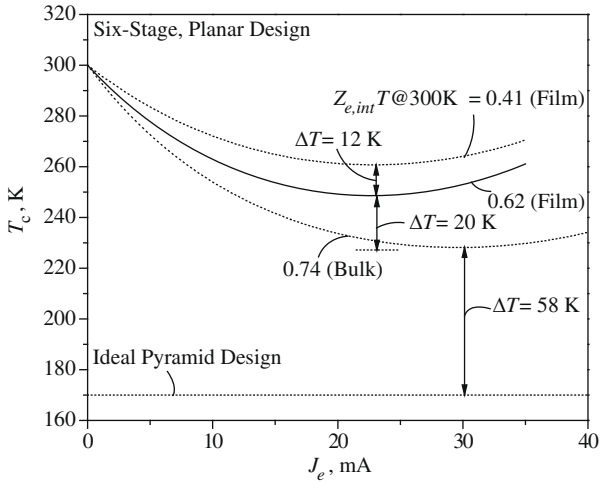

Fig. 9. Variation of the predicted cold stage temperatures for $Z_{e,int}T$ (T = 300 K) values of 0.41 (film using bulk k = 1.5 W/m K) [15], 0.62 (film using fitted film k = 1.0 W/m K), and 0.74 (bulk) [3], as a function of input current.

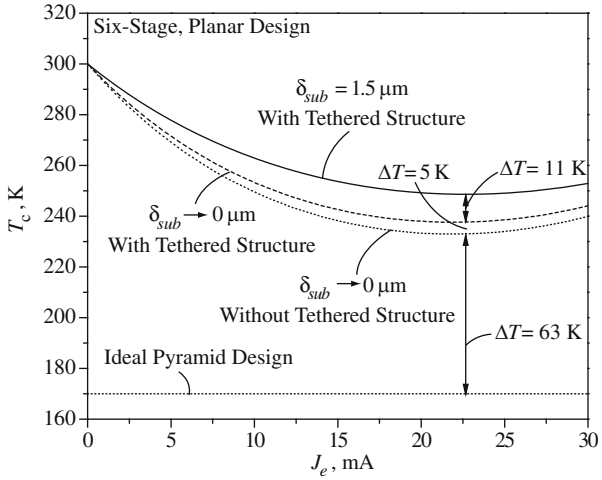

Fig. 10. Variation of cold stage temperature for δ_{sub} = 0 and 1.5 μm with respect to input current. The effect of glass tether is also shown.

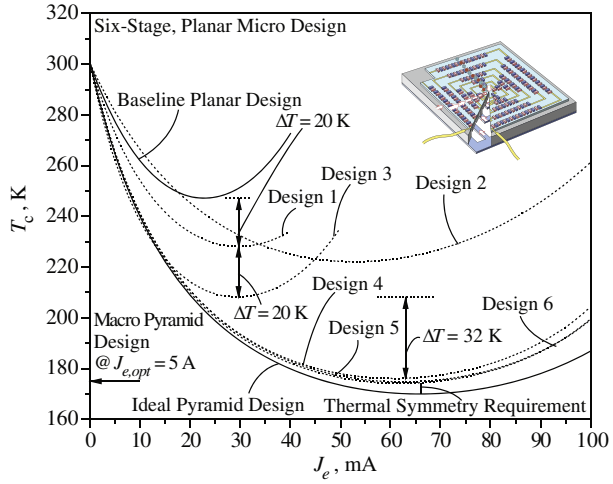

Fig. 8. Variation of the cold stage temperature with respect to input current, for baseline planar design, ideal pyramid design, and the six design designations described in Table 5. The cold stage temperature of a six-stage macro cooler using bulk TE elements is also shown at current of 5 A, which is close to that of the ideal pyramid design.

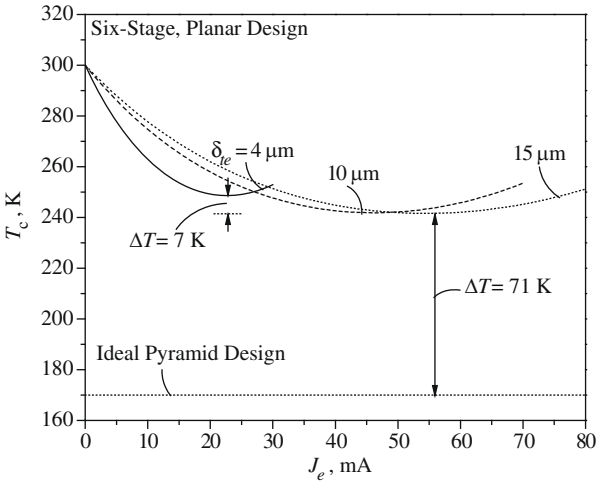

Fig. 11. Variation of cold stage temperature with respect to input current for δ_{te} = 4, 10, 15 μm, and with given δ_{sub} = 1.5 μm.

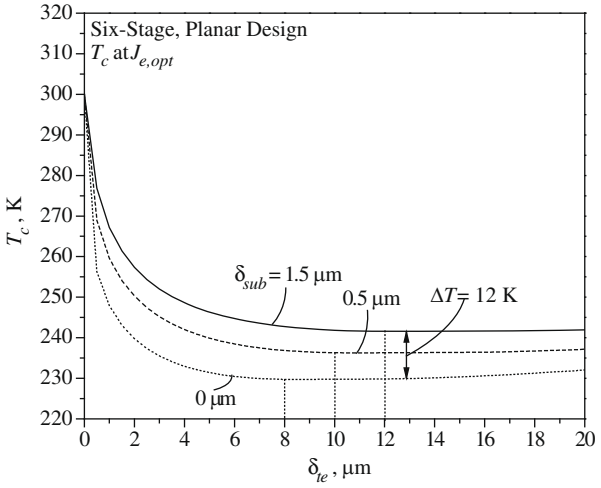

Fig. 12. Variation of cold stage temperature with respect to TE film thicknesses for δ_{sub} = 0, 0.5 and 1.5 μm. For δ_{sub} = 0, the glass tether is also removed. Other design parameters are kept the same as the baseline planar design.

Table 6
Significance of material-geometry selections on Seebeck coefficient, thermal conductivity, electrical resistivity, and electrical and thermal resistances.

	α_S	$k(R_{k,te})$	$R_{k,sub}$	$R_{k,tether}$	$\rho_e(R_{e,te})$	$R_{e,wire}$
(a) Figure of Merit $Z_{e,int}T$	○	○			○	
(b) TE film geometry		○			○	
(c) Substrate and tether			○	○		
(d) Electrical Wires						○

thickness, which indicates optimal TE film thickness decreases when we can remove the substrate.

5. Conclusions

A planar six-stage micro TE cooler is designed for cooling to low temperatures under vacuum, and a thermal network model is developed to investigate the optimal cooling performance considering interfacial thermal/electrical transport and temperature-dependent TE material properties. With the measured TE film properties, $Z_{e,int}T$ (T = 300 K) = 0.62 and the current fabrication constraints, the optimal six-stage micro TE cooler design predicts ΔT_{max} = 51 K with a power consumption of 68 mW, while the predicted performance of the five-stage prototype agrees well with the on-going experimental results.

The performance is influenced by (a) TE film quality $Z_{e,int}T$ (figure of merit), i.e., high α_S, low k, and low ρ_e, (b) optimal TE film structure $R_{k,te}$ and $R_{e,te}$), (c) maximum thermal isolation of the substrate structure $R_{k,sub}$ and tether structure $R_{k,tether}$, and (d) minimum electrical resistance of wires $R_{e,wire}$. These criticality of each parameter is summarized in Table 6.

Further improvements can be achieved by

(a) improving TE film quality $Z_{e,int}T$ (using supperlattice [22], or alloy/doping [23]),
(b) optimizing TE film geometry (i.e., aspect ratio, Section 4.2),
(c) increasing thermal isolation of substrate (i.e., removing the substrate and tether [17]),
(d) minimizing inter-connecting electrical wires, (e.g., using high electrical conductive material Au, Ni, Al, or large cross-section area [17]).

The interfacial effects and radiation gains show minor effects. Without the inherent disadvantages of the planar micro TE cooler, the maximum temperature difference will be increased by nearly 2.6-fold.

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